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MULTIPLE TWIN CELL NON-VOLATILE MEMORY ARRAY AND LOGIC BLOCK STRUCTURE AND METHOD THEREFOR

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BACKGROUND

[1001] The present invention relates to non-volatile memory array structures, and in preferred embodiments, particularly relates to those suitable for implementation of both memory and logic block structures.

[1002] Ongoing developments in semiconductor processing technologies and memory cell technologies continue to increase the density achieved in integrated circuit memory arrays. For example, certain passive element memory cell arrays may be fabricated having word lines approaching the minimum feature size (F) and minimum feature spacing for the particular word line interconnect layer, and also having bit lines approaching the minimum feature width and minimum feature spacing for the particular bit line interconnect layer. Moreover, three-dimensional memory arrays having more than one plane or level of memory cells have been fabricated implementing such so-called $4F^2$ memory cells on each memory plane. Exemplary three-dimensional memory arrays are described in U.S. Patent No. 6,034,882 to Johnson, entitled "Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication," and in U.S. Patent No. 5,835,396 to Zhang, entitled "Three-Dimensional Read-Only Memory."

[1003] A variety of other memory cell technologies and arrangements are also known. For example, NAND flash and NROM flash EEPROM memory arrays are also known to achieve relatively small memory cells. Other small flash EEPROM cells are known which use hot electron programming, such as NROM and floating gate NOR flash memory arrays. Such memory cells may also be desirable for a 3D memory array, although they frequently use many masks to produce a memory layer,

and some use relatively high programming currents. Moreover, Ferro-electric (FeRAM) memory arrays are also known to produce relatively small memory cells.

SUMMARY

[1004] The availability of extremely dense memory cell structures, and particularly those implemented in a three-dimensional memory array, provides an opportunity for new array structures for implementing memory and logic functions.

[1005] In an exemplary embodiment, a memory array includes X-lines or word lines, and further includes Y-lines or bit lines, with a memory cell associated at each intersection of a word line and a bit line. Individual memory cells are typically programmed by selecting, during a program mode, a single word line and bit line. During a read mode, however, a group of word lines is simultaneously driven to access a group of memory cells associated with a bit line. Various types of memory cells may be used which, when selected, add to the bit line current, such as passive element cells and EEPROM cells, as well as others. A true bit line and a complement bit line may be simultaneously selected, and coupled to a sense amplifier circuit.

[1006] Such a memory array structure may be used to compensate for the failure of a particular memory cell to program, by programming other memory cells along the same bit line and which are associated with the selected word line group. In addition, a virgin bit failure or other similar defect in a memory cell associated with one of the bit lines may be compensated by programming multiple memory cells associated with the complement bit line. Moreover, even if implemented using write-once memory cells, such a memory array may be "re-written" by programming at least one more cell associated with the opposite bit line group than the number of previously programmed memory cells associated with one bit line group. This capability is particularly advantageous for arrays containing trim information or other configuration information that might benefit from the ability to rewrite each location a few times, even when the underlying cell technology is non-erasable.

[1007] Memory array structures in accordance with the present invention may be used to implement a variety of logic functions by using multiple program cycles of memory cells on each bit line, thereby adjusting the amount of aggregate memory cell

current which flows on the bit line. In various configurations, a non-volatile content addressable memory array may be achieved. In other configurations, an array may be configured to perform threshold logic, and weighted threshold logic.

[1008] In some exemplary embodiments of the invention, a non-volatile array includes a first plurality of X-lines configured to be logically identical in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line. Each of the first plurality of X-lines may also be associated with a second Y-line group numbering at least one Y-line. In some embodiments, the first and second Y-Line groups are simultaneously selectable in a read mode and, when so selected, are respectively coupled to true and complement inputs of a sense amplifier circuit. Such Y-line groups may number only one Y-line, or may number more than one Y-line.

[1009] In some embodiments, such as certain ones in which the first and second Y-line groups each numbers more than one Y-line, a reference signal may be operably coupled to either the true or complement input of the sense amplifier circuit. Such a reference signal may comprise a reference current in some embodiments.

[1010] In some embodiments, the first Y-line group includes more than one Y-line, and each of the first Y-line group is configured to be logically identical in a read mode of operation. In many embodiments, each of the first plurality of X-lines is configured to be logically independent in a write mode of operation.

[1011] A wide variety of memory cells are contemplated for use with the invention. Passive element memory cells, especially anti-fuse memory cells, are particularly contemplated, but magnetoresistive passive element memory cells and EEPROM memory cells are contemplated as well. Moreover, the invention is well suited for use in both two-dimensional arrays and three-dimensional arrays. In embodiments using a three-dimensional array technology, the first plurality of X-lines may be disposed on more than one layer of the array, or may be disposed on a single layer of the array.

[1012] The invention in various embodiments may be configured to store data as in a traditional memory arrangement, may be configured to perform threshold logic

upon one or more inputs to the array, and may be configured as a content addressable memory array.

[1013] The invention in several aspects is suitable for integrated circuits having an array, for cell and array structures, for methods for operating such integrated circuits and array structures, and for computer readable media encodings of such integrated circuits or array structures, all as described herein in greater detail and as set forth in the appended claims.

[1014] The foregoing is a summary and thus contains, by necessity, simplifications, generalizations and omissions of detail. Consequently, those skilled in the art will appreciate that the foregoing summary is illustrative only and that it is not intended to be in any way limiting of the invention. Other aspects, inventive features, and advantages of the present invention, as defined solely by the claims, may be apparent from the detailed description set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

[1015] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[1016] Fig. 1 depicts a non-volatile memory array in accordance with certain embodiments of the present invention, in which individual word lines are selected during programming, but multiple word lines are selected for reading.

[1017] Fig. 2 depicts a graph of bit line current as a function of the number of programmed memory cells which might be simultaneously selected on a bit line group.

[1018] Fig. 3 depicts the bit line current for a multiple twin cell arrangement.

[1019] Fig. 4 is a graph showing three levels of programmed current, corresponding to different numbers of programmed cells.

[1020] Fig. 5 is a graph showing the spread of bit line current for "n" programmed cells and for "n+1" programmed cells, illustrating the tightening achieved by programming multiple cells.

[1021] Fig. 6 depicts a memory array structure which includes a respective plurality of bit lines that are collectively coupled to a respective input of a sense amplifier, where both of the two bit line groups are associated with the selected group of word lines.

[1022] Fig. 7 illustrates an advantageous use of the structure shown in Fig. 6, in which a group of memory cells associated with one bit line group are programmed to compensate for a virgin bit failure which occurs on a memory cell associated with the other bit line group.

[1023] Fig. 8 illustrates an advantageous use of the structure shown in Fig. 6, in which a group of memory cells associated with a bit line group are programmed to compensate for a failure to program another memory cell associated with the same bit line group.

[1024] Fig. 9 depicts a memory array structure in which an input to a second word line decoder is a complementary signal relative to an input to a first word line decoder, which structure provides for any of four different logic functions which may be implemented in the array.

[1025] Fig. 10 depicts a non-volatile content addressable memory (NVCAM) implemented using a similar memory array structure.

[1026] Fig. 11 depicts a memory array which is configured to perform threshold logic and weighted threshold logic, in which the weights are non-volatile and are set by multiple program cycles of many different memory cells.

[1027] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION

[1028] Referring to Fig. 1, a non-volatile memory array 100 is depicted in accordance with certain embodiments of the present invention, in which individual word lines are selected during programming, but multiple word lines are selected for reading. The exemplary memory array 100 includes a row decoder 102 for generating a plurality of row select output signals R1, R2, R3, ... RN, which are respectively conveyed to word line decoders 104, 106, 108, 110. Each word line decoder receives a row select signal and drives four word lines. For example, word line decoder 104 is responsive to row select signal R1 and generates four word lines WL1, WL2, WL3, WL4. During programming, one of the four word lines 105 is selected at any one time (responsive to decode signals not shown), whereas during read mode all four word lines 105 are simultaneously selected in response to R1.

[1029] Other groups of word lines (also referred to herein as "X-lines") are also depicted. Word line decoder 106 is responsive to row select signal R2 and generates four word lines WL5, WL6, WL7, WL8 of word line group 107. Word line decoder 108 is responsive to row select signal R3 and generates four word lines WL9, WL10, WL11, WL12 of word line group 109. Lastly, word line decoder 110 is responsive to row select signal RN and generates four word lines WL13, WL14, WL15, WL16 of word line group 111. Each word line decoder is configured, like decoder 104, to select one of its four word lines during programming and select all four of its word lines during read mode. Since row decoder 102 generates one active row select signal, during read only one word line group of four word lines is selected, and during programming only one word line itself is selected.

[1030] Two pairs of bit lines (also referred to herein as "Y-lines") are depicted, each being selected by a respective column select signal. Bit lines BL1, BL2 are respectively coupled by select devices 123, 124 to signal buses 127, 128 when selected by a COLSEL1 signal generated by column decoder 122. Similarly, bit lines BL3, BL4 are respectively coupled by select devices 125, 126 to signal buses 127, 128 when selected by a COLSEL2 signal. A data sensing circuit 129 generates a DATAOUT signal based upon the signal coupled to signal buses 127, 128.

[1031] In the memory array 100, a memory cell is represented at each intersection of a word line and a bit line. Such memory cells may include 2-terminal passive element memory cells, and may include other programmable memory cells, such as 3-terminal EEPROM cells, as described below in greater detail, although only a single X-line and Y-line is depicted for each memory cell location (i.e., other types of wires for certain memory cell types are not shown).

[1032] To understand the operation of this exemplary array, assume that the array includes antifuse passive element memory cells, and that the X-lines are driven and the Y-lines are sensed. Further assume that word lines WL5, WL6, WL7, and WL8 of word line group 107 are selected and that bit lines BL1 and BL2 are selected by COLSEL1. A group of 8 memory cells (labeled as 130) are thus selected during such a read cycle. Four of the selected memory cells are associated with BL1, and the other four memory cells are associated with BL2. To program a logic "1" into the selected group of cells 130 within the array 100, one or more memory cells associated with BL2 are programmed, and no memory cells associated with BL1 are programmed. To read this data, the cell current flowing on bit line BL2 results from one or more programmed cells, while the cell current flowing on bit line BL1 arises just from leakage current through the four unprogrammed cells associated with bit line BL1. To program a logic "0" into the cells 130, one or more memory cells associated with BL1 is programmed, and no memory cells associated with BL2 are programmed. To read this data, the cell current flowing on bit line BL1 results from one or more programmed cells, while the cell current flowing on bit line BL2 is the leakage current through the four unprogrammed cells associated with bit line BL2. No reference signal is required, for the leakage current flowing on one bit line essentially forms the reference signal for the other bit line.

[1033] Thus far, similar operation could have been achieved by a twin cell arrangement in which each bit of data is stored in true and complement form in two respective memory cells. However, by configuring the array so that multiple word lines are selected during read mode, numerous advantages may be achieved. For a memory cell technology in which the programmed cell current varies widely, additional cells may be programmed to ensure that a certain minimum "cell current" (actually, an aggregate cell current of the simultaneously selected cells which flows

on the bit line) is achieved, even if one or more of the programmed cells has an unusually low value of programmed current. Since no mid-level reference signal is required, the circuit is very resistant to noise, and the available signal is doubled compared to having a reference level corresponding to the midpoint between the programmed and unprogrammed value of cell current. Moreover, by programming up to four memory cells on either the true or complement bit lines, the signal achieved is 8X greater than the worst case signal achieved when using the mid-level reference. This is true for either a stored one or a stored zero.

[1034] This advantage is illustrated in Fig. 2 and Fig. 3. Referring now to Fig. 2, a graph of the bit line current is depicted as a function of the number of programmed memory cells which are simultaneously selected on a bit line. The region 150 corresponds to none of the memory cells being programmed, and the upper limit of this region, labeled as 152, represents the maximum leakage current on the bit line. The region 156 represents the bit line current resulting from one memory cell being programmed, and the lower limit of this range, labeled 162, represents the minimum bit line current. A reference level 164 is traditionally generated at the mid-point between these two levels of current, which allows the bit line current to be compared to the reference level to determine the data state of the cell being read. Accordingly, the sense amplifier threshold has a value set by the difference between the reference level 164 and the maximum leakage level 152 (shown as threshold 166), and also by the difference between the reference level 164 and the minimum programmed current level 162. Also shown in the figure, the region 158 represents the bit line current corresponding to two programmed memory cells, and the region 160 represents the bit line current corresponding to three programmed memory cells. Such additional current cannot be discriminated when the reference level is set as indicated in the figure.

[1035] Referring now to Fig. 3, the bit line currents for a multiple twin cell arrangement is depicted. As before, region 150 corresponds to none of the memory cells being programmed, and the upper limit of this region, labeled as 152, represents the maximum leakage current on the bit line. The region 178 may be viewed as representing the bit line current resulting from one memory cell being programmed, and the lower limit of this range, labeled 174, represents the minimum programmed

bit line current. Since the bit line current for one bit line is compared to the bit line current for the other bit line, the sense amplifier threshold has a value set by the difference between the minimum programmed current 174 and the maximum leakage level 152, shown as threshold 176. This results in a doubling of the sense amplifier threshold level.

[1036] However, when additional memory cells are potentially programmed, the minimum programmed current 174 may increased to a higher value, which increases the sense amplifier threshold even more than the factor of two described above. Assuming each programmed memory cell linearly added to bit line current, programming four such memory cells would result in a sense amplifier threshold which is a factor of eight higher than the sense amplifier threshold 166 shown in Fig. 2. Even assuming some variation in the magnitude of each cell's programmed current, the minimum programmed current 174 may be assured of increasing when more than one memory cell is programmed, with a resultant improvement of the sense amplifier threshold which is achieved. In some embodiments, a read-after-write verification operation may be performed to determine the number of memory cells to program to achieve a desired minimum programmed current on a bit line.

[1037] In addition, the arrangement depicted in Fig. 1 is frequently tolerant of a "virgin bit failure," which is an unprogrammed memory cell which nonetheless is conductive (or at least very leaky) due to a manufacturing defect. For example, if memory cell 131 is conductive as manufactured, a logic one can be easily written into the locations 130 by programming one or more additional memory cells associated with BL2, which merely reinforces the current through memory cell 131. However, to program a logic zero, several memory cells associated with BL1 may be programmed, which together generate a greater bit line read current than the leaky cell 131, and thus can be sensed as a logic zero by the sense circuit 129.

[1038] The array structure depicted in Fig. 1 may also be used to store more than one bit of data within the memory cell group 130 rather than just one bit, as described above. Referring now to Fig. 4, a graph is depicted showing three levels of programmed current, corresponding to none programmed (region 202), 1 cell programmed (region 204), and two cells programmed (region 206). By using multiple

program cycles (e.g., for some embodiments, on more than one memory cell, and for other embodiments, multiple programming cycles on a single cell), the distribution of programmed currents may be tightened, especially those cells having widely varying programmed currents. In such embodiments, a reference level could be set to a level above the current corresponding to N-cells programmed, and the programming of the cells could be controlled using a feedback scheme to continue programming until the desired level of programmed current is achieved. By tightening the programming spread, the magnitude of the spread can be less than the reference spread I_{REF} between adjacent programmed values, as shown in Fig. 5. The region 210 corresponds to the spread of bit line current for "n" programmed cells, while the region 212 corresponds to the spread of bit line current for "n+1" programmed cells. By increasing the difference between these two spreads 210 and 212, a reference level 208 generated at the mid-point between such spreads will provide a larger sense amplifier threshold value, depicted as 214.

[1039] The same general memory array structure as described above may be used as a logic block, rather than as a more typical memory block, to implement threshold logic and weighted input threshold logic. Since this kind of logic block replaces fairly complex logic gates, one can afford to utilize many inexpensive memory cells. As before, such a structure is based on the ability to adjust the strength of an input by virtue of the multiple memory cells that are simultaneously selected during a read mode operation.

[1040] In the above examples, a group of word lines are configured as logically identical during a read mode of operation to access a group of memory cells, half of which are associated with a first selected bit line, and the other half associated with a second selected bit line, which two bit lines are respectively coupled to respective inputs of a selected sense amplifier. Referring now to Fig. 6, a memory array structure 220 is depicted which expands this concept to include a respective plurality of bit lines that are collectively coupled to a respective input of a sense amplifier. Both of these two bit line groups are associated with the selected group of word lines, and thus a memory cell is disposed at the intersection of each word line and bit line.

[1041] The exemplary memory array 220 includes two input signals WLIN1, WLIN2, such as from a row decoder (not shown), which are respectively conveyed to word line decoders 222, 224. In typical practice it should be understood that many more such word line decoders may be implemented, but for clarity only two are depicted here. Each word line decoder receives an input signal and drives four word lines. Word line decoder 222 generates a group 232 of four word lines WL1, WL2, WL3, WL4. During programming, one of these four word lines 232 is selected at any one time (responsive to decode signals not shown), whereas during read mode all four word lines 232 are simultaneously selected (assuming, of course, that the input signal WLIN1 is selected). Similarly, word line decoder 224 generates a group 233 of four word lines WL5, WL6, WL7, WL8. For the present description, assume that only one input signal WLIN1, WLIN2, is active at any time, and that consequently, only one word line group of four word lines is selected during read mode of operation, and only one word line itself is selected during programming mode.

[1042] Two groups 234, 235 of bit lines are depicted. During a read operation, both such bit line groups 234, 235 are simultaneously selected by a respective column select signal (not shown) and coupled to respective inputs of a sense amplifier circuit 230. Bit lines BL1, BL2, BL3, and BL4 are collectively coupled to signal bus 228, and bit lines BL5, BL6, BL7, and BL8 are collectively coupled to signal bus 229. A reference signal is also coupled to the signal bus 229 by a signal generator 231 (e.g., such as a current source). The two signal buses 228, 229 are coupled to respective inputs of the sense amplifier 230, which then generates a read data signal. The sense amplifier 230 may be shared by other non-selected bit line groups (not shown). As with the word line decoders, the bit line decoders 226, 227 select one bit line for programming, but simultaneously select all four bit lines during read. Suitable decoder and programming circuitry may be incorporated depending upon the technology employed in manufacturing the memory array, and no particular advantage is believed afforded by any one circuit form, at least in the context of practicing this invention.

[1043] As before, a memory cell is represented at each intersection of a word line and a bit line. Such memory cells may include 2-terminal passive element memory cells, and may include other programmable memory cells, such as 3-terminal

EEPROM cells, as described below in greater detail, although only a single X-line and Y-line is depicted for each memory cell location (i.e., other types of wires for certain memory cell types are not shown). Preferably such memory cells are passive element memory cells, and more preferably they are antifuse cells.

[1044] As may be appreciated, a single input such as WLIN1 causes four word lines to be selected during a read mode, which drives sixteen memory cells coupled to the non-inverting input of a selected sense amplifier, and which also drives another sixteen memory cells coupled to the inverting input of the selected sense amplifier. The bit line currents on each of the bit lines within bit line group 234 are summed together before sensing, as are the four bit line currents within bit line group 235. As may be appreciated, the strength of a single input may be varied greatly, depending upon how many of the sixteen memory cells in group 236 are programmed, and depending upon how many of the sixteen memory cells in group 237 are programmed. This may be utilized to achieve a tighter distribution of aggregate I_{CELL} current.

[1045] The memory array 220, even if implemented using write-once memory cells (e.g., certain anti-fuse memory cells), may be "re-written" by programming at least one more cell associated with one bit line group (e.g., group 236) than the number of previously programmed memory cells associated with the other bit line group (e.g., group 237). For example, the memory location defined by groups 236 and 237 may be initially programmed to a logic "1" state by programming one memory cell within group 236. Later, the memory location may be re-written to a logic "0" by programming two cells within group 237. Even later, the memory location can be re-written back to a logic "1" by programming two more cells within group 236 (for a total of three programmed cells). Alternatively, the number of programmed cells in each step could be larger to increase the sense amplifier threshold. This capability is particularly advantageous for arrays containing trim information or other configuration information that might benefit from the ability to rewrite each location a few times, even when the underlying cell technology is non-erasable.

[1046] The next several figures illustrate several other advantageous uses of such a memory array structure. In Fig. 7, a group of memory cells 241 (e.g., here shown as

a group of six such cells) associated with one bit line group 234 are programmed to compensate for a virgin bit failure 240 which occurs on a memory cell associated with the other bit line group 235. The aggregate bit line current flowing in bit line group 234 overcomes the aggregate bit line current resulting from the virgin bit failure 240 which flows in bit line group 235.

[1047] In Fig. 8, a group of memory cells 262 (e.g., here shown as a group of two such cells) associated with bit line group 235 are programmed to compensate for a failure to program cell 261 associated with the same bit line group 235. With sixteen such memory cells associated with both the word line group 232 and the bit line group 235, a wide range of programmed current may be achieved, and may compensate for the failure of one or a few such cells to program.

[1048] In Fig. 9, a memory array structure 280 is depicted which is identical with that shown in Figs. 6, 7, and 8 except that the input 284 to the second word line decoder 224 is a complementary signal relative to the input 282 to the first word line decoder 222. Consequently, during a read mode the group of logically identical word lines 232 is complementary to the group of logically identical word lines 233. In the figure, a pair of word line decoders is depicted which respectively receive true and complement versions of a single input signal 282. It should be appreciated that in actual practice a number of such complementary pairs of word line decoders may be provided, each associated with a respective input signal, and each associated with at least one group of bit lines. As illustrated in the figure, each bit line group numbers more than one bit line (e.g., here shown as four bit lines in each group), but each such bit line group may number as few as a single bit line.

[1049] Each of the four groups of memory cells shown performs a particular logic function of the input 282. Each of the memory cells in group 292 (i.e., the group of sixteen memory cells representing the word line/bit line intersections between word line group 232 and bit line group 234) performs an OR function; while each of the memory cells in group 293 performs a NOR function; each of the memory cells in group 294 performs a NAND function; and each of the memory cells in group 295 performs an AND function. Since there are sixteen memory cells within each of these four groups, the weight of each input may be varied widely by programming a

particular number of the memory cells within a group. By including a number logic inputs, complicated weighted logic functions may be implemented in a space efficient manner.

[1050] Such a structure just described may be utilized to implement a non-volatile content-addressable memory array (NVCAM). Referring now to Fig. 10, a NVCAM 350 is depicted which receives a digital word on an input bus 351 and generates a series of outputs 362 on a match bus 356 for each detected pattern. A programmable AND array 354 is provided for each desired match pattern, and which generally follows the arrangement depicted in Fig. 9. An X-line decoder 352 receives the input data word and generates true and complement versions of each bit position, which are then conveyed to the array blocks 354 as groups of at least one logically identical X-lines associated with each such true and complement signal. Two such groups 358, 360 are depicted.

[1051] Referring now to Fig. 11, a memory array 400 is depicted which is configured to perform threshold logic and weighted threshold logic. In this case the weights are non-volatile and are set by multiple program cycles of many different memory cells. The first word line decoder 222 receives a first arbitrary input signal INPUT1 while a second word line decoder 224 receives another arbitrary input signal INPUT2, which would typically be unrelated to INPUT1. As with the other embodiments described herein, only a portion of a memory array expected in practice is depicted in the figure and described herein, as many instantiations of such word line decoders would be anticipated, each associated with a respective one of a much larger of logic input signals.

[1052] In operation, the logic value output which is generated by sense amplifier 230 is a weighted function of each input which is either added to, or subtracted from, an accumulated total for the bit line groups 234 and 235. For example, each programmed memory cell within the memory cell group 402 incrementally adds bit line current to the aggregated signal on bit line group 234. Depending upon the number of memory cells so programmed, a factor of from 0 to 16 times the logic signal INPUT1 may be added to the bit line group 234 aggregate current. Since this

bit line group 234 is coupled to the *non-inverting* input of sense amplifier 230, such increased current performs an ADD function.

[1053] In contrast, each programmed memory cell within the memory cell group 404 incrementally adds bit line current within bit line group 235. Depending upon the number of memory cells so programmed, a factor of from 0 to 16 times the logic signal INPUT1 may be added to the bit line group 235 aggregate current. Since this bit line group 235 is coupled to the *inverting* input of sense amplifier 230, such increased current performs a SUBTRACT function.

[1054] Such a weighted logic block structure uses far fewer gates than implementations using more basic logic functions, such as AND, OR, INVERT, and XOR. For example, a parity tree grows linearly when implemented as weighted threshold logic, rather than growing as an N^2 polynomial. Moreover, the relative advantage of such a weighted threshold logic family grows with increasing numbers of input signals. The "cost" of this logic function may be measured as the number of crosspoints within each group, and very inexpensive crosspoint cells may be converted into a high logic computational power.

[1055] The weights of each input may be programmed into the non-volatile array, which may be implemented as a write-once antifuse memory array, or as a write-many (i.e., re-writable) device. While such an array is slow to program, and likely relatively slow in execution when compared to combinatorial logic, it has a great density advantage, particularly when the number of logic inputs is high.

[1056] The array structures described herein may also be utilized with memory cell structures other than passive element memory cells. For example, when an EEPROM memory cell technology is used, multiple program cycles may be used to adjust the threshold of a programmed memory cell until a desired magnitude of bit line current is achieved. Similarly, such memory cells may be programmed to achieve one of several desired magnitudes of bit line current, and thus can provide for storing more than one data bit within a group of cells, and can provide for an enhanced weighted threshold logic structure.

[1057] In the various descriptions herein, memory cells are frequently described as being individually programmed by selecting a single word line and single bit line, while during a read mode a group of word lines are configured to be logically identical so that more than one memory cell may contribute to bit line (or bit line group) current. It is also contemplated, however, that more than one memory cell may be programmed simultaneously in some embodiments of the present invention. For example, two memory cells which are associated with a given word line may be simultaneously programmed if two bit lines are simultaneously selected. Such two bit lines may be disposed within the same bit line group (i.e., for read mode) or may be disposed in different bit line groups.

[1058] As used herein, a "group" of objects may include a plurality of such objects, but need only include at least one, but not necessarily more than one. Moreover, an integrated circuit having a three-dimensional memory array is assumed to be a monolithic integrated circuit, rather than an assembly of more than one monolithic integrated circuit. The methods and apparatus of the present invention may also be used to advantage in monolithic three dimensional memories such as, for example, a three-dimensional, non-volatile, field-programmable memory array (both write-once and/or re-writable memory arrays). In such embodiments, the various word lines of a group of simultaneously selected word lines may be all located on the same layer of the array, or may be located on several different layers of word lines (i.e., associated with more than one memory plane of memory cells). Moreover, the methods and apparatus of the present invention may also be used to advantage in integrated circuits including two-dimensional arrays, and in many other non-memory integrated circuits.

[1059] Preferably, the memory cells are comprised of semiconductor materials, as described in U.S. Patent 6,034,882 to Johnson et al., U.S. Patent 5,835,396 to Zhang, U.S. Patent 6,420,215 to Knall, and U.S. Patent 6,515,888 to Johnson, et al., each of which are hereby incorporated by reference. Specifically an antifuse memory cell is preferred. Other types of memory arrays, such as MRAM and organic passive element arrays, can also be used. MRAM (magnetoresistive random access memory) is based on magnetic memory elements, such as a magnetic tunnel junction (MTJ). MRAM technology is described in "A 2556kb 3.0V ITIMTJ Nonvolatile

Magnetoresistive RAM" by Peter K. Naji et al., published in the Digest of Technical Papers of the 2001 IEEE International Solid-State Circuits Conference, ISSCC 2001/Session 7/Technology Directions: Advanced Technologies/7.6, February 6, 2001 and pages 94-95, 404-405 of ISSCC 2001 Visual Supplement, both of which are hereby incorporated by reference. Certain passive element memory cells incorporate layers of organic materials including at least one layer that has a diode-like characteristic conduction and at least one organic material that changes conductivity with the application of an electric field. U.S. Patent No. 6,055,180 to Gudensen et al. describes organic passive element arrays and is also hereby incorporated by reference. Memory cells comprising materials such as phase-change materials and amorphous solids can also be used. See U.S. Patent No. 5,751,012 to Wolstenholme et al. and U.S. Patent No. 4,646,266 to Ovshinsky et al., both of which are hereby incorporated by reference.

[1060] The methods and apparatus of the present invention may also be used to advantage in other monolithic three dimensional memories, such as those described in Johnson et al., U.S. Patent No. 6,034,882, "Vertically-Stacked, Field Programmable, Nonvolatile-Memory and Method of Fabrication"; Johnson, U.S. Patent No. 6,525,953, "Vertically-Stacked, Field Programmable, Nonvolatile-Memory and Method of Fabrication"; Knall et al., U.S. Patent No. 6,420,215, "Three Dimensional Memory Array and Method of Fabrication"; Lee et al., U.S. Patent Application No. 09/927,648, "Dense Arrays and Charge Storage Devices, and Methods for Making Same," filed August 13, 2001; Herner et al., U.S. Patent Application No. 10/326,470, "An Improved Method for Making High Density Nonvolatile Memory," filed December 19, 2002; Walker et al., U.S. Patent Application No. 10/335,089, "Method for Fabricating Programmable Memory Array Structures Incorporating Series-Connected Transistor Strings," filed December 31, 2002; Scheuerlein et al., U.S. Patent Application No. 10/335,078, "Programmable Memory array Structure Incorporating Series-Connected Transistor Strings and Methods for Fabrication and Operation of Same," filed December 31, 2002; Cleeves, U.S. Patent Application No. 10/185,508, "Three Dimensional Memory," filed June 27, 2002; Kleveland, et al., U. S. Patent Application No. 09/897,705, "Three-Dimensional Memory Array Incorporating Serial Chain Diode Stack," filed June 29, 2001; and Johnson, U.S.

Patent Application No. 10/185,208, "Low-cost, Serially-Connected, Multi-Level Mask-Programmable Read-Only Memory," filed June 27, 2002; all assigned to the assignee of the present invention and hereby incorporated by reference.

[1061] As used herein, a passive element memory array includes a plurality of 2-terminal memory cells, each connected between an associated X-line and an associated Y-line. Such a memory array may be a two-dimensional (planar) array or may be a three-dimensional array having more than one plane of memory cells. Each such memory cell has a non-linear conductivity in which the current in a reverse direction (i.e., from cathode to anode) is lower than the current in a forward direction. Application of a voltage from anode to cathode greater than a programming level changes the conductivity of the memory cell. The conductivity may decrease when the memory cell incorporates a fuse technology, or may increase when the memory cell incorporates an antifuse technology. A passive element memory array is not necessarily a one-time programmable (i.e., write once) memory array.

[1062] Such passive element memory cells may generally be viewed as having a current steering element directing current in a direction and another component which is capable of changing its state (e.g., a fuse, an antifuse, a capacitor, a resistive element, etc.). In certain preferred embodiments of the present invention, the memory element is a diode-like structure having a p+ region separated from an n– region by an antifuse element. When the antifuse element is programmed, the p+ region is electrically connected to the n– region and forms a diode. In an organic PEMA embodiment, the memory element is a diode-like structure having an anode region separated from a cathode region by an organic material layer whose conductivity changes as electrons are injected into the layer.

[1063] As used herein, a memory array does not necessarily imply a fully-decoded array configured to access data stored at each addressable location, although certain embodiments described herein do contemplate such a memory array. Rather, a memory array refers to an array of memory cells, even if the array is configured to implement a logic function quite unlike a fully decoded traditional memory array.

[1064] Word lines may also be referred to as row lines or X-lines, and bit lines may also be referred to as column lines or Y-lines. The distinction between "word"

lines and "bit" lines may carry certain connotations to those skilled in the art. When reading a memory array, it is assumed by some practitioners that word lines are "driven" and bit lines are "sensed." Moreover, the memory organization (e.g., data bus width, number of bits simultaneously read during an operation, etc.) may have some association with viewing one set of the two array lines more aligned with data "bits" rather than data "words." Neither connotation is necessarily required in this description, although neither is inconsistent with at least some embodiments described.

[1065] The directionality of X-lines (e.g., which may be shown horizontally) and Y-lines (e.g., which may be shown vertically) is merely convenient for ease of description of the two groups of crossing lines in the array. While X-lines are usually orthogonal to Y-lines, such is not necessarily implied by such terminology.

[1066] Integrated circuits incorporating a memory array usually subdivide the array into a sometimes large number of smaller arrays, also sometimes known as sub-arrays. As used herein, an array is a contiguous group of memory cells having contiguous word and bit lines generally unbroken by decoders, drivers, sense amplifiers, and input/output circuits. An integrated circuit including a memory array may have one array, more than one array, or even a large number of arrays. An used herein, an integrated circuit memory array is a monolithic integrated circuit structure, rather than more than one integrated circuit device packaged together or in close proximity, or die-bonded together.

[1067] Based upon the teachings of this disclosure, it is expected that one of ordinary skill in the art will be readily able to practice the present invention. The descriptions of the various embodiments provided herein are believed to provide ample insight and details of the present invention to enable one of ordinary skill to practice the invention. Although certain supporting circuits (e.g., decoders, sensing circuits, multiplexers, input/output buffers, etc.) are not specifically described, such circuits are well known, and no particular advantage is afforded by specific variations of such circuits in the context of practicing this invention. Moreover, it is believed that one of ordinary skill in the art, equipped with the teaching of this disclosure, will be able to carry out the invention, including implementing various control circuits

inferred but not specifically described herein, using well known circuit techniques and without undue experimentation. Nonetheless, additional details of bias conditions, bias circuits, and layer decoder circuits particularly suitable for a three-dimensional memory array of write-once anti-fuse passive element memory cells are described in U.S. Patent 6,618,295 to Roy E. Scheuerlein, entitled "Method and Apparatus for Biasing Selected and Unselected Array Lines When Writing a Memory Array", and in "Three-Dimensional Memory Array Incorporating Serial Chain Diode Stack" by Kleveland, et al, U.S. Patent Application No. 09/897,705, filed on June 29, 2001, which are both hereby incorporated by reference in their entirety. Moreover, useful row and column circuits are described in "Multi-Headed Decoder Structure Utilizing Memory Array Line Driver with Dual Purpose Driver Device," U. S. Patent Application No. 10/306,887, filed November 27, 2002, and in "Tree Decoder Structure Particularly Well Suited to Interfacing Array Lines Having Extremely Small Layout Pitch," U. S. Patent Application Serial No. 10/306,888, filed November 27, 2002, which applications are hereby incorporated by reference in their entirety.

[1068] The block diagrams herein may be described using the terminology of a single node connecting the blocks. Nonetheless, it should be appreciated that, when required by the context, such a "node" may actually represent a pair of nodes for conveying a differential signal, or may represent multiple separate wires (e.g., a bus) for carrying several related signals or for carrying a plurality of signals forming a digital word.

[1069] While circuits and physical structures are generally presumed, it is well recognized that in modern semiconductor design and fabrication, physical structures and circuits may be embodied in computer readable descriptive form suitable for use in subsequent design, test or fabrication activities as well as in resultant fabricated semiconductor integrated circuits. Accordingly, claims directed to traditional circuits or structures may, consistent with particular language thereof, read upon computer readable encodings and representations of same, whether embodied in media or combined with suitable reader facilities to allow fabrication, test, or design refinement of the corresponding circuits and/or structures. The invention is contemplated to include circuits, related methods or operation, related methods for making such circuits, and computer-readable medium encodings of such circuits and methods, all

as described herein, and as defined in the appended claims. As used herein, a computer-readable medium includes at least disk, tape, or other magnetic, optical, semiconductor (e.g., flash memory cards, ROM), or electronic medium and a network, wireline, wireless or other communications medium. An encoding of a circuit may include circuit schematic information, physical layout information, behavioral simulation information, and/or may include any other encoding from which the circuit may be represented or communicated.

[1070] The foregoing detailed description has described only a few of the many possible implementations of the present invention. For this reason, this detailed description is intended by way of illustration, and not by way of limitations. Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope and spirit of the invention. Moreover, the embodiments described above are specifically contemplated to be used alone as well as in various combinations. It is only the following claims, including all equivalents, that are intended to define the scope of this invention. Accordingly, other embodiments, variations, and improvements not described herein are not necessarily excluded from the scope of the invention.